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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,638	09/29/2004	Kazuhiro Umemoto	JP920030236US1	5637

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EXAMINER	
SEMENENKO, YURIY	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 08/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,638	UMEMOTO, KAZUHIRO	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/04/04page1*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1.1. Claims 1 and 3 are rejected under 35U.S.C. 103(a) as being obvious over Applicant's Reference hereinafter "ApRef" in view of Washino (Patent # 5484963 hereafter "Washino").

1.1.1. Regarding claim 1: Applicant discloses in Fig. 1 of the "Background of the invention" section, multilayer wiring board 1 adapted to receive a semiconductor chip 5 to be soldered thereto, comprising: an insulating layer 2; a plurality of electrode pads 3 provided on said insulating layer 2 so that each of said electrode pads is located corresponding to an associated one of a plurality of solder bumps 4 of the semiconductor chip to be soldered ; a solder resist 6

covering said insulating layer 6 and said electrode pads 3; openings provided in said solder resist covering said electrode pads, each of said openings reaching a surface of the electrode pad; and solder 4 filled into the openings of said solder resist, each of the openings of said solder resist is smaller than said oblong shape (see Fig. 1),

except, Applicant's reference doesn't explicitly teach each of the electrode pads corresponding to the solder bumps located near an outer periphery of the semiconductor chip to be soldered has an oblong shape, and a center of said opening is located to be offset from a center of said oblong shape in a direction toward a center of the semiconductor chip to be soldered.

Washino teaches in Fig. 5 each of the electrode pads 13 corresponding to the solder bumps located near an outer periphery of the semiconductor chip to be soldered has an oblong shape, and a center of said opening is located to be offset from a center of said oblong shape in a direction toward a center of the semiconductor chip to be soldered. Therefore, at time the invention was made, it was well know to use each of the electrode pads corresponding to the solder bumps located near an outer periphery of the semiconductor chip to be soldered has an oblong shape, and a center of said opening is located to be offset from a center of said oblong shape in a direction toward a center of the semiconductor chip to be soldered.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made for ApRef. to include in his invention each of the electrode pads corresponding to the solder bumps located near an outer periphery of the semiconductor chip to be soldered has an oblong shape, and a center of said opening is located to be offset from a center of said oblong shape in a direction toward a center of the semiconductor chip to be soldered,as taught by because Washino teaches such structure can tolerate a positional variation of each of pads for constituting connecting terminals.

1.1.2. Regarding claim 3: Applicant discloses in Fig. 1 of the "Background of the invention" section, multilayer wiring board 1 with a semiconductor chip 5 mounted thereon, comprising: an insulating layer 2; a plurality of electrode pads 3 on said insulating layer; a solder resist 6 cover said insulating layer 2 and said electrode pads 3; openings provided in said solder resist covering said electrode pads, each of said openings reaching a surface of the electrode pad; the

semiconductor chip 5 having a plurality of electrodes each arranged to correspond to an associated one of said electrode pads; and solder joints 4 filling said openings, respectively, each of said solder joints connecting the corresponding one of said electrode pads to the corresponding one of said electrodes of said semiconductor chip 5, wherein each of the openings of said solder resist 6 is smaller than said oblong shape,

except, Applicant's reference doesn't explicitly teach each of the electrode pads corresponding to the electrodes located near an outer periphery of said semiconductor chip has an oblong shape, and a center of said opening is located to be offset from a center of said oblong shape in a direction toward a center of said semiconductor chip.

Washino teaches in Fig. 5 each of the electrode pads 13 corresponding to the electrodes located near an outer periphery of said semiconductor chip has an oblong shape, and a center of said opening is located to be offset from a center of said oblong shape in a direction toward a center of said semiconductor chip.Therefore, at time the invention was made, it was well know to use each of the electrode pads corresponding to the electrodes located near an outer periphery of said semiconductor chip has an oblong shape, and a center of said opening is located to be offset from a center of said oblong shape in a direction toward a center of said semiconductor chip.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made for ApRef. to include in his invention each of the electrode pads corresponding to the electrodes located near an outer periphery of said semiconductor chip has an oblong shape, and a center of said opening is located to be offset from a center of said oblong shape in a direction toward a center of said semiconductor chip, as taught by because Washino teaches such structure can tolerate a positional variation of each of pads for constituting connecting terminals.

1.2. Claims 2 and 4 are rejected under 35U.S.C. 103(a) as being obvious over Applicant's Reference hereinafter "ApRef" in view of Washino and in view of Masayuki (Patent # JP-09-102517 hereafter "Masayuki".

1.2.1. Regarding claims 2 and 4: Applicant, as modified, discloses in Fig. 1 of the "Background of the invention" section, multilayer wiring board having all of the claimed features as discussed

above with respect claim 1 (3), wherein each of the electrode pads corresponding to the solder bumps located near said outer periphery has an oval shape,

except, Applicant's reference doesn't explicitly teach each of the openings of said solder resist has a circular shape.

Masayuki teaches (Fig. 4 and [0003]) each of the openings of the solder resist has a circular shape. Therefore, at time the invention was made, it was well know how to make each of the openings of the solder resist has a circular shape.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made for ApRef. to include in his invention each of the openings of said solder resist has a circular shape.

Benefit of doing so to cover electrical pad by insulator.

2.1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

2.2. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)- 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

8.3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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RANDY W GIBSON
PRIM[illegible]ER